

REMARKS

In response to the Office Action mailed May 18, 2005, Applicants respectfully request reconsideration. To further the prosecution of this Application, Applicants submit the following remarks, have canceled claims and have added new claims. The claims as now presented are believed to be in allowable condition.

Claims 1-24 were pending in this Application. By this Amendment, claims 20-24 have been canceled without prejudice. Applicants expressly reserve the right to prosecute at least some of the canceled claims and similar claims in one or more related Applications. Claims 25-32 have been added. Accordingly, claims 1-19 and 25-32 are now pending in this Application. Claims 1, 11, 16 and 19 are independent claims.

Election/Restriction

Claims 1-24 were subject to a restriction requirement under 35 U.S.C. §121. In particular, claims 1-19 (Group I) were deemed to be drawn to a printed circuit board. Claims 20-24 (Group II) were drawn to a method of fabricating a circuit board.

The Office Action references a prior telephone conversation with Applicant's Representative, David E. Huang, in which Mr. Huang elected Group I without traverse. Applicant hereby affirms the election of Group II without traverse, namely, claims 1-19.

Rejections under §102 and §103

Claims 1-3, 8-9, 11 and 12 were rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,519,580 (Natarajan et al.). Claims 4, 5, 10, 13 and 15 were rejected under 35 U.S.C. §103(a) as being unpatentable over Natarajan et al. in view of U.S. Patent No. 6,201,305 (Darveaux et al.). Claim 6 was rejected under 35 U.S.C. §103(a) as being unpatentable over Natarajan et al. in view of U.S. Publication No. 2002/0071935 (Wu). Claims 7 and 14 were

rejected under 35 U.S.C. §103(a) as being unpatentable over Natarajan et al. in combination with Wu, and in further view of U.S. Patent No. 5,844,782 (Fukasawa). Claims 16, 18 and 19 were rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,847,936 (Forehand et al.) in view of Natarajan et al. Claim 17 was rejected under 35 U.S.C. §103(a) as being unpatentable over Forehand et al. in view of U.S. Patent No. 6,194,782 (Katchmar).

Applicants respectfully traverse each of these rejections and request reconsideration. The claims are in allowable condition because they patentably distinguish over the prior art.

Natarajan discloses an integrated circuit package 10 housing an integrated circuit 12 such as a microprocessor, and having a plurality of solder balls 14 that extend from the bottom of the package surface 16 (column 2, lines 34-39 and Fig. 1). The package 10 has a plurality of solder landings dedicated to power 18p, ground 18g and signals 18s (column 2, lines 49-53 and Fig. 2). The solder landings are coupled to the integrated circuit 12 by internal wire routing and vias 20 that extend into the body of the package 10 (column 2, lines 53-55). The soldered landing 18s also has a plurality of conductive tabs 26 that symmetrically extend from a center area 28 of the landing 18s (column 2, lines 61-63 and Fig. 3). The bottom surface of the package 10 is covered with a solder mask 32 which has a plurality of openings 34 that expose the solder landings 18 (column 3, lines 7-9). The openings 34 have a diameter that is larger than the diameter of the center areas of the landings 18 (column 3, lines 9-11). The solder balls 36 are reflowed and allowed to harden (column 3, lines 27-28 and Fig. 6). The symmetric tabs 26 allow equal symmetric solder flow across the center area so that there is created a symmetric uniform solder joint (column 3, lines 32-33). The package 10 is typically mounted to a printed circuit board 40 which has a plurality of conductive surface pads 42 arranged in the same pattern as the solder landings 18 (column 3, lines 41-44 and Fig. 7).

Darveaux discloses a mounting pad 28 including at least two spokes 32 extending outward from it in a radial direction (column 6, lines 14-17 and Figs. 3A and 3B). It is desirable that the centroid of the pad 28, i.e., the area of the central pad 14 and spokes 32 exposed by the circular opening 22 in an insulative mask 20, be coincident with the centroid opening (column 6, lines 42-48).

Wu discloses a solder pad 2 formed in a radial-shape contour on an upper surface of a substrate 1 (paragraph 0021 and Figs. 6A, 6B and 8). A radial-shaped opening 32 surrounds the solder pad 2 and exposes the top surface thereof (paragraph 0021 and Figs. 6A, 6B and 8).

Fukasawa discloses lands 16 whose external diameter D2 is 0.6 mm, whose pattern protecting film 17 opening diameter D1 is set to 0.75 mm, and whose gap of over 0.05 mm is thereby provided between the pattern-protecting film 17 and each of the lands 16 (column 3, lines 28-32 and Fig. 3A). In this way, gaps are always formed between external electrodes 13 formed on the lands 16 by heating and melting solder grains or solder paste or the like and the pattern-protecting film around them (column 33-39). Consequently, even when a temperature cycle test or the like is carried out, the external electrodes 13 and the pattern-protecting film 17, the thermal expansion coefficient of which are greatly different, are kept out of contact with each other and consequently thermal stresses do not act in the base portions of the external electrodes 13 as has happened in devices of the related art of this kind (column 3, lines 40-46).

Forehand discloses a packaged integrated circuit 201 and a printed circuit board (PCB) 220 (column 2, lines 45-47 and Fig. 1). Interconnects layers 241 and 242 are patterned to provide a plurality of electrically conductive traces which are connected to the PCB signal via plugs 223-225 (column 4, lines 24-28 and Fig. 3).

Katchmar discloses, as a high density package design, a surface mount area-array package (column 1, lines 18-19). Katchmar further discloses BGAs and a CCGA (Figs. 4, 5, 6 and 7).

Claims 1-10

Claim 1 is directed to a pad layout for mounting with a circuit board component. The pad layout includes a set of pads arranged on a surface of a circuit board in a two-dimensional array having at least two pads in a first direction and at least two pads in a second direction that is substantially perpendicular to the first direction. Each pad of the set of pads has (i) a central portion and (ii) multiple lobe portions integrated with the central portion and extending from the central portion of that pad.

Natarajan does not teach or suggest a pad layout for mounting with a circuit board component, where the pad layout includes a set of pads arranged on a surface of a circuit board, as recited in claim 1. Rather, Natarajan discloses an integrated circuit package 10 housing an integrated circuit 12 such as a microprocessor (e.g., see column 2, lines 34-39 and Fig. 1 of Natarajan).

"A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference."<sup>1</sup> "The identical invention must be shown in as complete detail as is contained in the ... claim."<sup>2</sup> Since each and every element of claim 1 is not found in Natarajan, the rejection of claim 1 under 35 U.S.C. §102(b) in view of Natarajan is improper.

For the reasons stated above, claim 1 patentably distinguishes over the cited prior art, and the rejection of claim 1 under 35 U.S.C. §102(b) should be withdrawn. Accordingly, claim 1 is in allowable condition.

Because claims 2-10 depend from and further limit claim 1, claims 2-10 are in allowable condition for at least the same reasons.

Additionally, it should be understood that the dependent claims recite additional features which further patentably distinguish over the cited prior art. For example, claim 5 imposes limitations that where each pad of the set of pads

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<sup>1</sup> *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

<sup>2</sup> *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

has a profile having multiple outer radii of substantially 3 mils, and multiple concave radii of substantially 8 mils. These features are not taught or suggested by any of the other cited references. For example, Darveaux which was cited as disclosing a mounting pad 28 including at least two spokes 32 extending outward from it in a radial direction (e.g., column 6, lines 14-17 and Figs. 3A and 3B of Darveaux), does not disclose any pads having multiple outer radii of substantially 3 mils or multiple concave radii of substantially 8 mils as recited in claim 5. The Office Action contends that the pad and spokes of Darveaux can vary widely depending on the particular application at hand and cites column 6, lines 31-41 of Darveaux). Applicants respectfully submit that this is an incorrect characterization of Darveaux in that this characterization implies that all aspects of the Darveaux geometry can vary widely. Darveaux does not say this. Precisely, Darveaux states that the "size of the opening 22, the central pad 14 and the spokes 32 can vary widely" (emphasis added). Darveaux then proceeds to provide various values for the diameter of the Darveaux opening 22, the central pad 14 and the spokes 32. There is nothing in Darveaux that teaches or suggests features of any radii of the Darveaux structure. Moreover, none of the other cited references provides such a disclosure. A utility of the radii recited in claim 5 is that such radii blend well to avoid sharp angled intersections, as described in the Specification on page 9, lines 4-6. If the rejection of claim 5 is to be maintained, Applicants respectfully request that it be pointed out with particularity specifically where Darveaux provides disclosure of such radii features.

#### Claims 11-15

Claim 11 recites a circuit board which includes a set of circuit board layers combined to form a rigid planar structure having an outer surface; and a pad layout configured to mount with a circuit board component. The pad layout includes a set of pads arranged on the surface of a circuit board in a two-dimensional array having at least two pads in a first direction and at least two

pads in a second direction that is substantially perpendicular to the first direction. Each pad of the set of pads has (i) a central portion and (ii) multiple lobe portions integrated with the central portion and extending from the central portion of that pad.

Natarajan does not disclose a circuit board having a pad layout which includes a set of pads arranged on the surface of a circuit board in a two-dimensional array, as recited in claim 11. Rather, as mentioned above in connection with claim 1, Natarajan discloses an integrated circuit package 10 housing an integrated circuit 12 such as a microprocessor.

Accordingly, claim 11 patentably distinguishes over the cited prior art for at least the same reasons as claim 1. Thus, the rejection of claim 11 under 35 U.S.C. §102(b) should be withdrawn, and claim 11 is in allowable condition.

Because claims 12-15 depend from and further limit claim 11, claims 12-15 are in allowable condition for at least the same reasons.

Furthermore, the dependent claims recite additional features which further patentably distinguish over the cited prior art. For instance, claim 13 imposes limitations that where each pad of the set of pads has a profile having multiple outer radii of substantially 3 mils, and multiple concave radii of substantially 8 mils. As mentioned above in connection with claim 5, these features are not taught or suggested by any of the other cited references. Accordingly, if the rejection of claim 13 is to be maintained, Applicants respectfully request that it be pointed out with particularity specifically where Darveaux provides disclosure of such radii features.

#### Claims 16-18

Claim 16 is directed to a circuit board assembly which includes a set of circuit board layers combined to form a rigid planar structure having an outer surface; and a pad layout including a set of pads arranged on the surface of a circuit board in a two-dimensional array having at least two pads in a first direction and at least two pads in a second direction that is substantially

perpendicular to the first direction. Each pad of the set of pads has (i) a central portion and (ii) multiple lobe portions integrated with the central portion and extending from the central portion of that pad. The circuit board assembly further includes a circuit board component mounted to the pad layout via a set of solder joints.

Natarajan does not disclose a circuit board assembly having a pad layout which includes a set of pads arranged on the surface of a circuit board in a two-dimensional array, as recited in claim 16. Rather, as mentioned above in connection with claim 1, Natarajan discloses an integrated circuit package 10 housing an integrated circuit 12 such as a microprocessor.

As a result, claim 16 patentably distinguishes over the cited prior art for at least the same reasons as claim 1. Therefore, the rejection of claim 16 under 35 U.S.C. §102(b) should be withdrawn, and claim 16 is in allowable condition.

Because claims 17-18 depend from and further limit claim 16, claims 17-18 are in allowable condition for at least the same reasons.

#### Claim 19

Claim 19 is directed to a circuit board assembly which includes a set of circuit board layers combined to form a rigid planar structure having an outer surface; and a pad layout including a set of pads arranged on the surface of a circuit board in a two-dimensional array having at least two pads in a first direction and at least two pads in a second direction that is substantially perpendicular to the first direction. Each pad of the set of pads having (i) a central portion and (ii) multiple lobe portions integrated with the central portion and extending from the central portion of that pad. The circuit board assembly further includes a circuit board component, and means for mounting the circuit board component to the set of pads of the pad layout.

Natarajan does not disclose a circuit board assembly having a pad layout which includes a set of pads arranged on the surface of a circuit board in a two-dimensional array, as recited in claim 19. Rather, as mentioned above in

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connection with claim 1, Natarajan discloses an integrated circuit package 10 housing an integrated circuit 12 such as a microprocessor.

Accordingly, claim 19 patentably distinguishes over the cited prior art for at least the same reasons as claim 1. As a result, the rejection of claim 19 under 35 U.S.C. §102(b) should be withdrawn, and claim 16 is in allowable condition.

#### Newly Added Claims

Claims 25-32 have been added and are believed to be in allowable condition. Claims 25-26 depend from claim 1. Claims 27-28 depend from claim 11. Claims 29-30 depend from claim 16. Claims 31-32 depend from claim 19. Support for claims 25, 27, 29 and 31 is provided within the Specification, for example, on page 9, line 12 through page 11, line 23. Support for claims 26, 28, 30 and 32 is provided within the Specification, for example, on page 7, line 11 through page 9, line 25. No new matter has been added.

#### Conclusion

In view of the foregoing remarks, this Application should be in condition for allowance. A Notice to this affect is respectfully requested. If the Examiner believes, after this Amendment, that the Application is not in condition for allowance, the Examiner is respectfully requested to call the Applicant's Representative at the number below.

Applicants hereby petition for any extension of time which is required to maintain the pendency of this case. If there is a fee occasioned by this Amendment, including an extension fee, that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 50-0901.

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If the enclosed papers or fees are considered incomplete, the Patent Office is respectfully requested to contact the undersigned collect at (508) 366-9600, in Westborough, Massachusetts.

Respectfully submitted,

A handwritten signature in black ink, appearing to read "D. E. Huang", is written over a horizontal line.

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